or more of steps 610, 620, 630, 640, 650, and 660 may be omitted. Any permutations, combinations or variations of the above order should be construed to be different embodiments within the scope of the present invention. Table 1 below illustrates some exemplary variations of the partitioning order in furtherance of the present invention.

IN THE CLAIMS

Please amend Claim 22 as follows:

22. (~~A~~mended) A method of constructing a scan chain comprising the steps of:

a) adding scan cells to a netlist description of an integrated circuit design having a plurality of clock domains, said scan cells being coupled serially together to form a first scan chain having a scan cell ordering;

b) partitioning said scan cells of said first scan chain into sets of scan cells and generating partitioning information indicative thereof, said step b) comprising the steps of:

b1) partitioning said scan cells of said first scan chain into sets according to the clock domain of said scan cells wherein scan cells of a given set share the same clock domain; and

b2) partitioning scan cells of said sets of step b1) into subsets according to edge sensitivity of said scan cells wherein scan cells of a given subset share the same edge sensitivity and the same clock domain; and

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c) constructing a second scan chain by breaking said scan cell ordering of said first scan chain and reordering said scan cells based on said partitioning information wherein only scan cells of a same set are allowed to be reordered.

Please amend Claim 24 as follows:

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24. (Amended) The method as described in Claim 23 wherein said first scan chain comprises a reconfigurable multiplexer positioned relative to the scan cells of said first scan chain and wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the relative positions of said scan cells to the reconfigurable multiplexer of said first scan chain wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same relative position to said reconfigurable multiplexer.

Please amend Claim 25 as follows:

25. (Amended) The method as described in Claim 23 wherein said first scan chain and said second scan chain each comprise a surrounding cone of logic and wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the respective surrounding cone logic of the scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same surrounding cone logic.

Please amend Claim 26 as follows:

26. (Amended) The method as described in Claim 23 wherein each of said first scan chain and said second scan chain comprise a switching time and wherein said step b) further comprises the step of partitioning scan cells of said subsets of step b2) into subsets according to the respective switching times of the scan chains wherein scan cells of a given subset share the same edge sensitivity, the same clock domain and the same power rail.